WHAT IS CLAIMED IS:

1. A reconfigurable detector comprising:

at least one array of a plurality of pixels, each of the plurality of pixels selected to receive and read-out an input; wherein the pixel array is divided into at least one pixel group for conducting a common predefined analysis, wherein each of the pixel groups is comprised of at least two pixels;

each of the plurality of pixels having a programmable circuitry, in communication therewith, each of said circuitry being programmed with a dynamically configurable user-defined function such that each of said circuitry receives the input from the selected pixel and outputs a modified input; and

a summing circuit in communication with the plurality of programmable circuits, said summing circuit designed to sum the modified inputs from the common pixel group in a single binning instruction to generate a scalar output for the pixel group.

2. The reconfigurable detector of claim 1, wherein the pixel array is a one-dimensional array.

3. The reconfigurable detector of claim 1, wherein the pixel array is a two dimensional array.

4. The reconfigurable detector of claim 1, wherein the input comprises a spectrum selected from the group consisting of samples of interest from flowing streams, bead assays, cells, tagged cells, and raster-scanned static samples.

5. The reconfigurable detector of claim 4, wherein the spectrum comprises fluorescence spectrum.

6. The reconfigurable detector of claim 4, wherein the spectrum comprises different light scattering angles from the

samples of interest.

7. The reconfigurable detector of claim 4, wherein the spectrum comprises different Fourier frequencies of an image from the samples of interest.

8. The reconfigurable detector of claim 4, wherein the spectrum comprises light spectrum.

9. The reconfigurable detector of claim 4, wherein the modification of the received input comprises cross-correlation of the received spectrum with the respective user defined function for each selected pixel.

10. The reconfigurable detector of claim 9, wherein the cross-correlation comprises simultaneously multiplying the received spectrum with the user-defined function for each selected pixel and serially summing the product to generate the single scalar output.

11. The reconfigurable detector of claim 1, wherein the array of the plurality of pixels comprises an active pixel sensor.

12 The reconfigurable detector of claim 1, wherein the user-defined function comprises a function to selectively pick out a spectrum of the desired target.

13. The reconfigurable detector of claim 12, wherein the user-defined function is determined by Partial Least Square (PLS) analysis followed by eigenvector rotation.

14. The reconfigurable detector of claim 1, wherein each pixel from the array of the plurality of pixels comprises a uniquely configured bandpass filter and a detector.

15. The reconfigurable detector of claim 1, wherein the read-out of the received input is placed in a dynamically addressable random access memory before the modification.

16. The reconfigurable detector of claim 1 wherein the detector has at least two pixel groups each having at least two pixels, and wherein each pixel group has a plurality of independent user defined functions associated therewith.

17. The reconfigurable detector of claim 1, wherein the programmable circuitry is integrated within the array of the plurality of pixels.

18. The reconfigurable detector of claim 1, wherein the programmable circuitry is separately arranged from the array of the plurality of pixels.

19. The reconfigurable detector of claim 1, wherein the programmable circuitries of the pixel group collectively comprise a user-defined function template and an inner product computational unit.

20. The reconfigurable detector of claim 19, wherein the array of the plurality of pixels, the user-defined function template, and the inner product computational unit are integrated on the same chip.

21. The reconfigurable detector of claim19, wherein the array of the plurality of pixels, the user-defined function template, and the inner product computational unit are integrated via connections between a plurality of chips.

22. The reconfigurable detector of claim 21, wherein the array of the plurality of pixels, the user-defined function template, and the inner product computational unit are

integrated via connections between a plurality of chips using bump bonding.

23. The reconfigurable detector of claim 21, wherein the array of the plurality of pixels, the user-defined function template, and the inner product computational unit are integrated via connections between a plurality of chips using 3-D chip integration.

24. The reconfigurable detector of claim 19, wherein the inner product computational unit performs inner product computation simultaneously during a signal integration time.

25. The reconfigurable detector of claim 19, wherein the inner product computational unit performs inner product computation prior to readout of the input.

26. The reconfigurable detector of claim 1 further comprising at least one of the circuits selected from the group consisting of digital control, timing logic, analog processing, and communication circuits.

27. A reconfigurable detector for simultaneously detecting a plurality of targets, the detector comprising:

at least one array of a plurality of pixels, each of the plurality of pixels selected to receive and read-out an input; wherein the pixel array is divided into at least one pixel group for conducting a common predefined analysis, wherein each of the pixel groups is comprised of at least two pixels;

each of the plurality of pixels having at least two programmable circuitries designed to simultaneously perform calculations to detect the plurality of targets, in communication therewith, each of said circuitries being programmed with a dynamically configurable user-defined function associated with a target species such that each of

said circuitries receives the input from the selected pixel and outputs a modified input; and

at least two summing circuits associated with the plurality of programmable circuitries and designed to simultaneously generate outputs representative of the plurality of targets, each of said summing circuits designed to sum the modified inputs from the associated one of the programmable circuitries to simultaneously generate a scalar output representative of the desired target.

28. The reconfigurable detector of claim 27, wherein the pixel array is a one-dimensional array.

29. The reconfigurable detector of claim 27, wherein the pixel array is a two dimensional array.

30. The reconfigurable detector of claim 27, wherein the input comprises a spectrum selected from the group consisting of samples of interest from flowing streams, bead assays, cells, tagged cells, and raster-scanned static samples.

31. The reconfigurable detector of claim 30, wherein the spectrum comprises fluorescence spectrum.

32. The reconfigurable detector of claim 30, wherein the spectrum comprises different light scattering angles from the samples of interest.

33. The reconfigurable detector of claim 30, wherein the spectrum comprises different Fourier frequencies of an image from the samples of interest.

34. The reconfigurable detector of claim 30, wherein the spectrum comprises light spectrum.

35. The reconfigurable detector of claim 27, wherein the array of the plurality of pixels comprises an active pixel sensor.

36 The reconfigurable detector of claim 27, wherein the user-defined function comprises a plurality of user-defined functions to selectively pick out the plurality of desired targets.

37. The reconfigurable detector of claim 36, wherein the user-defined function is determined by Partial Least Square (PLS) analysis followed by eigenvector rotation.

38. The reconfigurable detector of claim 27, wherein each pixel from the array of the plurality of pixels comprises at least two uniquely configured multi-dimensional bandpass filters.

39. The reconfigurable detector of claim 27, wherein the read-out of the received input is placed in a dynamically addressable random access memory before the modification.

40. The reconfigurable detector of claim 27 wherein the detector has at least two pixel groups each having at least two pixels, and wherein each pixel group has a plurality of independent user defined functions associated therewith.

41. The reconfigurable detector of claim 27, further comprising at least one of the circuits selected from the group consisting of digital control, timing logic, analog processing, and communication circuits.

42. The reconfigurable detector of claim 27, wherein the programmable circuitries are integrated within the array of the plurality of pixels.

43. The reconfigurable detector of claim 27, wherein the programmable circuitries are separately arranged from the array of the plurality of pixels.

44. The reconfigurable detector of claim 27, wherein the programmable circuitries of the pixel group collectively comprise at least two user-defined function templates and at least two inner product computational units , wherein each of the at least two programmable circuitries of each pixel in the pixel group is independently associated with one of the user-defined function templates and the inner product computational units.

45. The reconfigurable detector of claim 44, wherein the array of the plurality of pixels, the user-defined function templates, and the inner product computational units are integrated on the same chip.

46. The reconfigurable detector of claim 44, wherein the array of the plurality of pixels, the user-defined function templates, and the inner product computational units are integrated via connections between a plurality of chips.

47. The reconfigurable detector of claim 46, wherein the array of the plurality of pixels, the user-defined function templates, and the inner product computational units are integrated via connections between a plurality of chips using bump bonding.

48. The reconfigurable detector of claim 46, wherein the array of the plurality of pixels, the user-defined function templates, and the inner product computational units are integrated via connections between a plurality of chips using 3-D chip integration.

49. The reconfigurable detector of claim 44, wherein the inner product computational units perform inner product computation simultaneously during a signal integration time.

50. The reconfigurable detector of claim 44, wherein the inner product computational units perform inner product computation prior to readout of the input.

51. The reconfigurable detector of claim 44, wherein the user-defined function templates and the computational units are two-dimensional.

52. The reconfigurable detector of claim 27, wherein the at least two summing circuits, each of said summing circuits sequentially generates a single scalar output representative of the plurality of targets.